Frequency Divider With 50% Duty Cycle

DESCRIPTION

Background of Invention

[Para 1] 1. Field of the Invention

[Para 2] The present invention provides a frequency divider, and more particularly, a frequency divider for generating odd-number and even-number divided frequencies with a 50% duty cycle.

[Para 3] 2. Description of the Prior Art

[Para 4] Digital integrated circuits have been highly developed. Personal computers, mobile phones, digital watches, and calculators, for example, are applications of digital integrated circuits. A complex digital integrated circuit often includes a plurality of divided frequencies used to enable each device in the circuit to operate properly. For example, because a CPU and a RAM operate using different clocks, a computer system should provide different divided frequencies for the CPU and the RAM to keep synchronization.

[Para 5] Please refer to Fig.1, which illustrates a schematic diagram of a prior art frequency divider 10. The frequency divider 10 includes a comparator 12 and a counter 14. The comparator 12 compares a dividing number n with a count of the counter 14. When the dividing number n equals the count of the counter 14, the comparator 12 outputs a high-level square wave. The counter 14 outputs a sequence of counts according to rising edges of a reference

frequency F_{ref}, and is reset by the high-level square wave of the comparator 12, so as to output a sequence of count cycles S_{cn}. Therefore, the frequency divider 10 can output a one-n'th frequency F_{cn} with a closed loop formed by the comparator 12 and the counter 14. For example, when outputting a one-second frequency F_{c2}, the frequency divider 10 sets the sequence of count cycles S_{cn} of the counter 14 to be two counts for one cycle. As to operations of the frequency divider 10 when outputting one-second frequency F_{c2}, please refer to Fig.2, which illustrates a waveform diagram versus time sequence. In Fig.2, a count cycle Sc2 represents the two-count cycle provided by the counter 14. As mentioned above, the counter 14 is triggered by the rising edges of the reference frequency F_{ref}, so when the count of the counter 14 is 2, the comparator 12 outputs a high-level signal. Meanwhile, the counter 14 is reset with the high-level square waves provided by the comparator 12 for counting from 1 again. As a result, the frequency divider 10 can output the one-second frequency F_{c2} with a 50% duty cycle from the comparator 12.

[Para 6] However, when outputting a one-n'th frequency with an odd number n (such as 1/3, 1/5, and 1/7 frequencies), the output frequency F_{cn} of the prior art frequency divider 10 has asymmetric duty cycles. Please refer to Fig.3, which illustrates a waveform diagram of the prior art frequency divider 10 when outputting a one-third frequency F_{c3}. As mentioned above, the counter 14 is triggered with the rising edges of the reference frequency F_{ref}, so that when the count of the counter 14 is 3, the comparator 12 outputs a high-level signal. Meanwhile, the counter 14 is reset with the high-level square waves provided by the comparator 12 for counting from 1 again. As a result, the frequency divider 10 outputs the one-third frequency F_{c3} from the comparator 12 with about a 33% duty cycle, as shown in Fig.3.

[Para 7] For those systems operated in low frequency bands, as long as all devices in the systems are triggered with either rising edges of the frequency F_{cn} or falling edges of the frequency F_{cn}, the asymmetric frequency F_{cn} of the prior art frequency divider 10 does not affect the systems. However, in high-

frequency or high-speed applications, some devices in a system are triggered with the rising edges of the frequency F_{cn}, and the other are triggered with the falling edges, so the asymmetry of the frequency F_{cn} will cause a serious problem in system synchronization. Although the frequency divider 10 can properly output 1/n frequencies having 50% duty cycles with even numbers n as shown in Fig.2, the frequency divider 10 should output 1/n frequencies with odd numbers n to a duty-cycle recovery unit for converting the asymmetric duty cycles to be symmetric duty cycles. Therefore, when a system needs both odd-number and even-number divided frequencies, the system should include an even-number frequency divider and an odd-number frequency divider with a duty-cycle recovery unit. However, owing to circuit limitations (such as inconsistence or noise), the duty-cycle of the odd-number frequency divider cannot completely convert asymmetries to symmetries. In short, the prior art frequency divider cannot output both even-number and odd-number divided frequencies using the same circuitry.

Summary of Invention

[Para 8] It is therefore a primary objective of the claimed invention to provide a frequency divider with a 50% duty cycle.

[Para 9] According to the claimed invention, a frequency divider with a 50% duty cycle includes: a bit shifter for outputting a first quotient, a second quotient and a remainder of the second quotient according to a dividing number; a counter for counting according to a reference frequency; a first comparator coupled to the bit shifter and the counter for outputting a first comparison result according to the first quotient and counts of the counter; a second comparator coupled to the bit shifter and the counter for outputting a second comparison result according to the second quotient and counts of the counter; a first flip flop coupled to the first comparator and the second comparator for outputting a first result according to the reference frequency,

the first comparison result, and the second comparison result; an AND gate coupled to the bit shifter and the first flip flop for outputting an AND result according to the remainder of the second quotient and the first comparison result; a second flip flop coupled to the AND gate for outputting a second result according to the AND result and the reference frequency; and an OR gate coupled to the first flip flop and the second flip flop for outputting a frequency according to the first result and the second result.

[Para 10] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[Para 11] Fig.1 illustrates a schematic diagram of a prior art frequency divider.

[Para 12] Fig.2 and Fig.3 illustrate waveform diagrams versus time when the frequency divider in Fig.1 outputs 1/2 and 1/3 frequencies.

[Para 13] Fig.4 illustrates a schematic diagram of a frequency divider with a 50% duty cycle.

[Para 14] Fig.5 illustrates a truth table of a JK flip flop.

[Para 15] Fig.6 illustrates a truth table of a D flip flop.

[Para 16] Fig.7 and Fig.8 illustrate waveform diagrams versus time when the frequency divider in Fig.4 outputs a 1/2 and a 1/3 frequencies.

Detailed Description

[Para 17] Please refer to Fig.4, which illustrates a schematic diagram of a frequency divider 20 with a 50% duty cycle in accordance with the present

invention. The frequency divider 20 includes a reference-frequency generator 22, a bit shifter 24, comparators 26 and 28, a counter 30, a JK flip flop 32, an AND gate 34, a D flip flop 36, an inverter (NOT gate) 38, and an OR gate 40. The reference-frequency generator 22 generates a reference frequency F for the counter 30, a terminal CK of the JK flip flop 32, and the inverter 38. The inverter 38 inverts the received reference frequency F to a terminal CK of the D flip flop 36. The bit shifter 24 outputs a dividing number n from a terminal Div1 to the comparator 26, a quotient of the dividing number n divided by 2 from a terminal Div2 to the comparator 28, and a remainder of the dividing number n divided by 2 from a terminal Cp2 to the AND gate 34. The counter 30 triggered by rising edges of the reference frequency F outputs counts starting from 1 to the comparator 26 and 28. The comparator 26 can compare the counts of the counter 30 with the dividing number n provided by the bit shifter 24. When a count of the counter 30 equals the dividing number n of the bit shifter 24, the comparator 26 outputs high-level signals to a terminal J of the JK flip flop 32 and the counter 30 for resetting the counter 30. By the same token, the comparator 26 can compare the counts of the counter 30 with the quotient of the dividing number n divided by 2 provided by the bit shifter 24. When a count of the counter 30 equals the quotient of the dividing number n divided by 2, the comparator 28 outputs high-level signals to a terminal K of the JK flip flop 32. Please refer to Fig.5, which illustrates a truth table of the JK flip flop 32. In Fig.5, "1" represents high-level signals, "0" represents low-level signals, J_n and K_n represent levels of signals received in the terminals J, K of the JK flip flop 32, Q_n represents a level of a signal outputted from a terminal Q of the JK flip flop 32, and Q_{n-1} represents the former status of signal levels outputted from the terminal Q. Therefore, according to the truth table in Fig.5, when an output signal of the comparator 26 in Fig.4 is low, and an output signal of the comparator 28 is high, the JK flip flop 32 outputs a high-level signal from the terminal Q, so the AND gate 34 performs an AND operation on the output signal of the terminal Q of the JK flip flop 32 and the remainder of the dividing number n divided by 2 provided by the terminal Cp2 of the bit shifter 24. Therefore, if both the remainder of the dividing number n divided by 2 and the output signal of the terminal Q of the JK flip flop 32 are 1, the

AND gate 34 outputs a high-level signal to the D flip flop 36. Please refer to Fig.6, which illustrates a truth table of the D flip flop 36. Similar to the notations used in Fig.5, in Fig.6, CK_n and D_n represent levels of input signals of the terminals CK and D of the D flip flop 36, while Q_n represents a level of output signals of the terminal Q of the D flip flop 36. Therefore, according to the truth table in Fig.6, if both the input signals of the terminals CK and D are high (when the reference frequency F is low, and when the output signal of the AND gate 34 is high), a high-level signal is outputted from the terminal Q of the D flip flop 36 to the OR gate 40. The OR gate 40 performs an OR operation on the output signals of the terminals Q of the D flip flop 36 and the JK flip flop 32, so as to output a 1/n frequency Fn of the reference frequency F.

[Para 18] Take a 1/2 frequency F2 for example, when outputting the 1/2 frequency F2, the present invention frequency divider 20 with the 50% duty cycle sets the dividing number n equal to 2 first. Then, please refer to Fig.7, which illustrates a waveform diagram versus time sequence of the frequency divider 20 when outputting the 1/2 frequency F2. In Fig.7, a waveform WF represents an waveform of the reference frequency F provided by the reference-frequency generator 22, a count CT2 represents the counts provided by the counter 30, waveforms W_{c1} and W_{c2} represent waveforms of output signals provided by the comparator 26 and 28, a waveform JK_Q represents a waveform of an output signal provided by the terminal Q of the JK flip flop 32, a waveform D_Q represents a waveform of an output signal provided by the terminal Q of the D flip flop 36, and a waveform WF_n represents a waveform of an output signal provided by the OR gate 40. As mentioned above, when outputting the 1/2 frequency F2, the present invention frequency divider 20 sets the dividing number n=2 for the bit shifter 24. The bit shifter 24 outputs the dividing number 2 to the comparator 26, the quotient (=1) of the dividing number 2 divided by 2 to the comparator 28, and the remainder (=0) of the dividing number 2 divided by 2 to the AND gate 34. The counter 30 triggered by the rising edges of the reference frequency F outputs the count CT2. The comparator 26 outputs high-level signals and the counter 30 is reset to count

from 1 when the count CT2 equals the dividing number 2. Similarly, the comparator 28 outputs high-level signals when the count CT2 equals 1. Then, the truth table of the JK flip flop 32 in Fig.5 is applied to the output signals of the comparator 26 and 28 for outputting the waveform JK_Q shown in Fig.7 from the Q terminal of the JK flip flop 32. Because the remainder of the dividing number 2 divided by 2 is 0, the output signals of the AND gate 34 is also 0 regardless of whether the output signals of the terminal Q of the JK flip flop 32 is high or low. That is, the input signal of the terminal D of the D flip flop 36 is 0 all the time in this case. Therefore, according to the truth table of the D flip flop 36 in Fig.6, the output signal of the terminal Q of the D flip flop 36 is low all the time (as the waveform D_Q shown in Fig.7). Finally, the OR gate 40 performs the OR operation on the output signals of the terminals Q of the JK flip flop 32 and the D flip flop 36, so as to output the waveform WF_n. The cycle of the waveform WF_n is two times the waveform WF, or the output signal of the OR gate 40 is the 1/2 frequency F2 of the reference frequency F with a 50% duty cycle.

[Para 19] By the same token, please refer to Fig.8, which illustrates a waveform diagram versus time sequence of the frequency divider 20 when outputting a 1/3 frequency F3. When outputting the 1/3 frequency F3, the frequency divider 20 sets the dividing number n equal to 3 for the bit shifter 24. The bit shifter 24 outputs the dividing number 3 to the comparator 26, the quotient (=1) of the dividing number 3 divided by 2 to the comparator 28, and the remainder (=1) of the dividing number 3 divided by 2 to the AND gate 34. The counter 30 triggered by the rising edges of the reference frequency F outputs the count CT3. The comparator 26 outputs high-level signals and the counter 30 is reset to count from 1 when the count CT3 equals the dividing number 3. Similarly, the comparator 28 outputs high-level signals when the count CT3 equals 1. Then, the truth table of the JK flip flop 32 in Fig.5 is applied to the output signals of the comparator 26 and 28 for outputting the waveform JK_Q shown in Fig.8 from the Q terminal of the JK flip flop 32. Because the remainder of the dividing number 3 divided by 2 is 1, the output

signals of the AND gate 34 is high when the output signal of the terminal Q of the JK flip flop 32 is high. The D flip flop 36 is triggered by the rising edges of the input signal of the terminal CK, or by the falling edges of the reference frequency F (because the reference frequency F is inverted by the inverter 38 for the terminal CK of the D flip flop 36), so according to the truth table of the D flip flop 36 in Fig.6, the output signal of the terminal Q of the D flip flop 36 is represented by the waveform D_Q shown in Fig.8. Finally, the OR gate 40 performs the OR operation on the output signals of the terminals Q of the JK flip flop 32 and the D flip flop 36, so as to output the waveform WF_n. The cycle of the waveform WF_n is three times the waveform WF, or the output signal of the OR gate 40 is the 1/3 frequency F3 of the reference frequency F with a 50% duty cycle.

[Para 20] In comparison, the present invention can output both odd-number and even number divided frequencies with the same circuit (as long as changing the dividing number n), and keep duty cycle symmetrical. Therefore, the present invention frequency divider with the 50% duty cycle improves problems of the prior art, and increases accuracy of the odd-number and even number divided frequencies, so as to maintain accurate operation of a system.

[Para 21] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.